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Conditional Access Module Hardware Brief

CA Module User Guide V0.2

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Reference

- [1] ISO/IEC 13818-1 Information technology – Generic coding of moving pictures and associated audio information: Systems
- [2] EN 50221:1997 Common interface specification for conditional access and other digital video broadcasting decoder applications.
- [3] PC Card Standard Volume 2 Electrical Specification Release 8.0
- [4] Philips LPC2212/LPC2214 Data sheet Rev. 01-02 February 2004 Preliminary.
- [5] Philips LPC2114/2124/2212/2214 User Guide 03 May 2003 Preliminary.
- [6] ETR 289 DVB Support for Use of scrambling and Conditional Access (CA) within digital broadcasting systems.

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CA Module Block Diagram

The following is a CA Module block diagram, where the grayed blocks are internal to the FPGA.

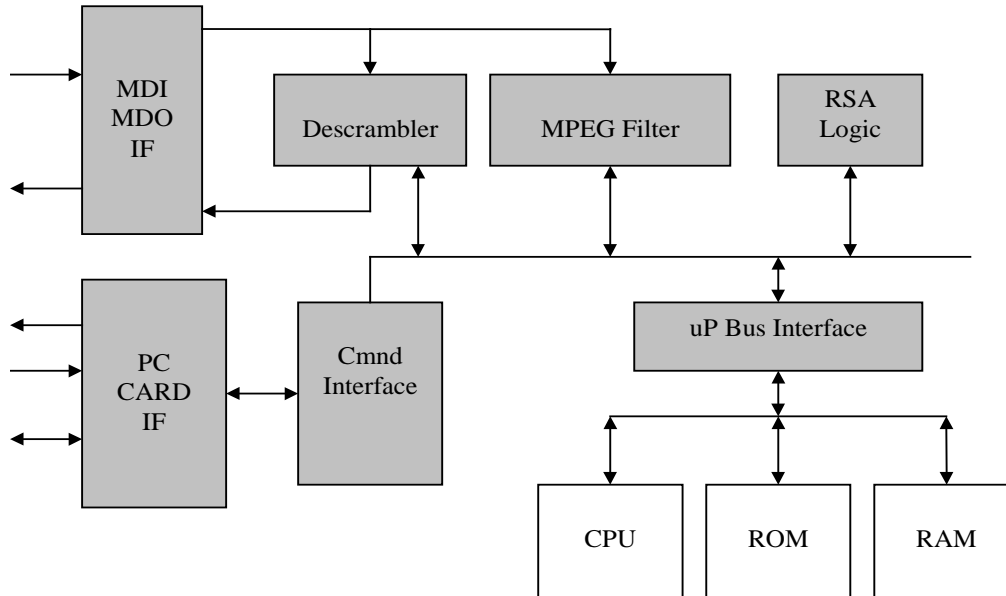


Figure 1

CA Module Pin List

The following table list all CA Module signals, divided into functional groups.

Signal Name	Direction	Description
N_CLR	In	Global asynchronous clear, active low (1)
PC Card specific		
D[7:0]	Bidir	PC Card Data Bus
A[11:0]	In	PC Card Address Bus
N_REG	In	Register select Active Low
N_WE	In	Write enable Active Low
N_OE	In	Output enable Active Low
N_IORD	In	I/O read Active Low
N_IOWR	In	I/O write Active Low
N_CE1	In	Card enable 1 Active Low
N_CE2	In	Card enable 2 Not Used
N_IOIS16	Out	16bit I/O Not Used (2)
N_WAIT	Out	Extend bus cycle Active Low (3)
N_INPACK	Out	Input port ack Active Low
N_IREQ	Out	Interrupt request Active Low (4)
N_DRV_EN	Out	External driver enable Active Low
MPEG in section		
MDI[7:0]	In	MP data in
MCLKI	In	MPEG-2 Clock input, running at 10MHz max
MISTRT	In	MP in Start flag
MIVAL	In	MP data in valid flag Active High
MPEG out section		
MDO[7:0]	Out	MP data out
MCLKO	Out	MPEG-2 Clock output running same frequency of MCLKI

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MOSTRT	Out	MP out start flag
MOVAL	Out	MP data out valid flag Active High
uP Interface		
UP_CLK	In	uP Clock running at 50 MHz (4)
UP_ADD[11:0]	In	uP Address Bus (6)
UP_DATA[15:0]	Bidir	uP Data Bus
N_UP_WE	In	uP Write enable Active Low
N_UP_CS	In	Chip Select Active Low
N_UP_OE	In	uP Output enable Active Low
N_EINT	Out	Interrupt request Active Low

1. Should driven directly by a uP general purpose I/O.
2. The PC Card IOIS16# is never asserted, should be connected to a pull up, as defined by [3]
3. Actually, the PC Card WAIT# is never asserted.
4. The PC Card Interrupt request is used as Ready
Is cleared to '0' after a N_CLR assertion.
Must be set to '1' by uP after full CIS memory programming
5. Address lines are intended as 16-bit word address.
In other words, the CA Module address A(0) is connected to the uP A(1) and so on for all other address lines

Table 1

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Microprocessor Interface

The Microprocessor Interface block controls all data transfer between the Ca Module and the uP, which is the Philips LPC2212/ LPC2214, based on 16/32 bit ARM7TDMI-S CPU core: see [4] and [5] for details. The CA Module uses the uP following signals: see [5] Table 3. Address lines are intended as 16-bit word address: refer for details to [5] PHILIPS UM_LPC2114_2124_2212_2214_2 user guide Figure 8: 16 Bit Bank External Memory Interfaces. In other words, the CA Module address A(0) is connected to the uP A(1).

Signal Name	Description
XCLK	Clock Output
A(11:0)	External Memory Address lines
D(15:0)	External memory data lines.
CS2	Low-active Chip Select 2 signal.
WE	Low-active Write enable signal.
OE	Low-active Output enable signal.
EINT0	External interrupt 0 input.

Table 2

Address Map

The Ca Module uses 12 uP address lines.

The most significant address lines are used to address the main internal functional block, while the remaining less significant address lines are used to select the configuration and status registers inside each block.

A(11:8)	Hex Address range	Block
0	000:0FF	General
1	100:1FF	Host Interface
2	200:2FF	PC Card Attribute Memory (CIS)
3	300:3FF	MPEG-2 Descrambler
4	--	--
5:6	--	--
7	700:7FF	MPEG-2 Filters register
8:F	800:FFF	MPEG-2 Filters data blocks

Table 3

General Register Description

Name	Mode	Offset	Bit	Field Name	Description
Global Inten	R/W	0	7:0		Main Interrupt Enable
			0	HINTEN	Host Interface Interrupt Enable
			1	FINTEN	Filters Interrupt Enable
			2	DSCRINTEN	Descrambler Interrupt Enable, not used
Global Status	R	1	7:0		Main Status register
			0	HINT	Host Interface Interrupt Request
			1	FINT	Filters Interrupt Request
			2	DSCRINT	Descrambler Interrupt Request
Rate Generator	W	2	15:0		Controls the Smart card SC_CLK output frequency
			7:0	N parameter	Pulses to be generated (1)
			15:8	M parameter	Period counter (1)
Version Number	R	2	15:0		HDL code Version Number
			15:0	Version Number	Integer, hardwired (2)

1. The output frequency generate is $(50\text{MHz} * N / M) / 2$.
2. Actual Version Number value is X"0001".

Table 4

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Please note that the above interrupt requests read by uP are ANDded by the correspondent enable signals.

Bus timing

The following figures the basic memory read and write cycles, extracted from [5].

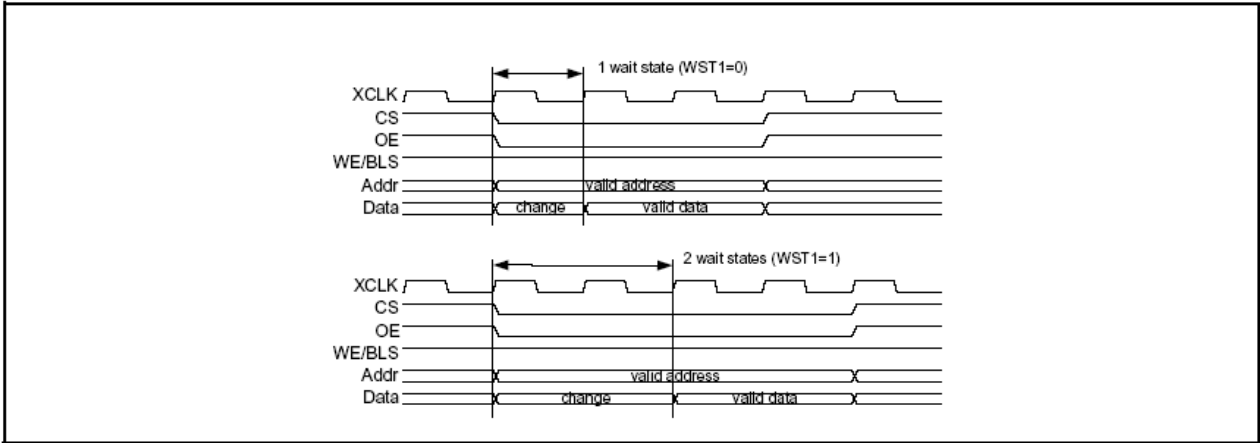


Figure 10: External memory read access (WST1=0 and WST1=1 examples)

Figure 2

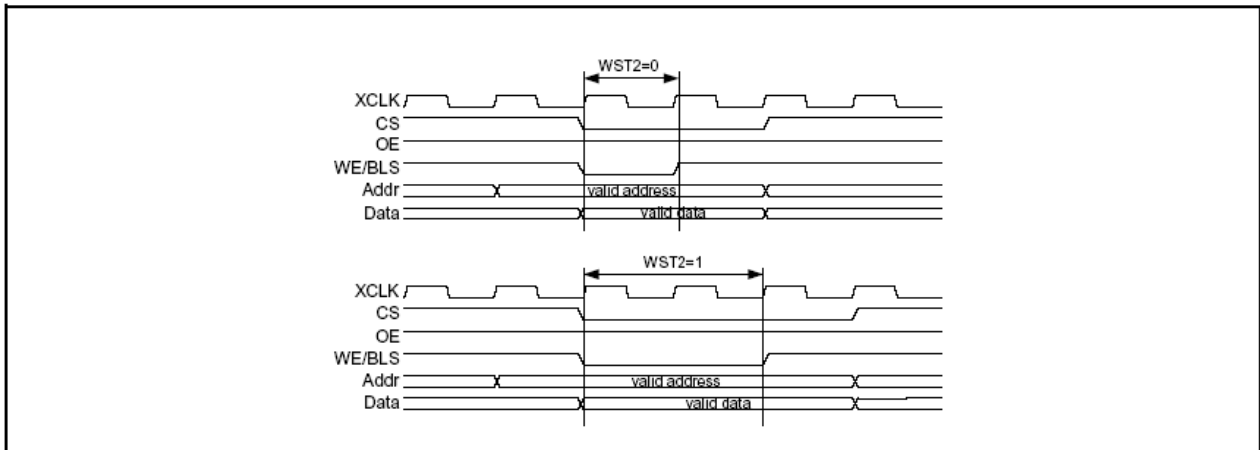


Figure 11: External memory write access (WST2=0 and WST2=1 examples)

Figure 3

The uP External Memory Controller must be programmed WST1 = 2 and WST2 = 1.

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HOST INTERFACE

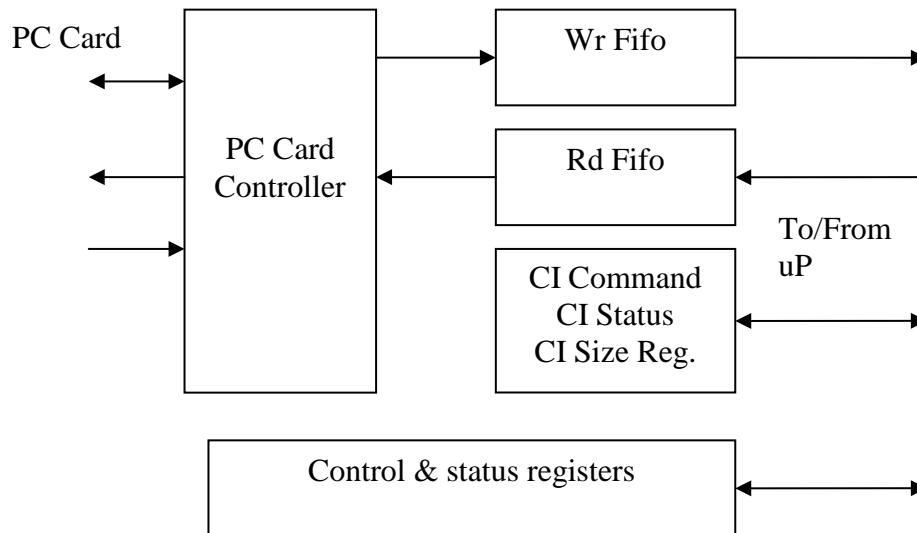


Figure 4

Host interface implements the Physical layer (PC card-based) of the Command Interface, as described by [2] Annex A. Only the Host to module (A.2.2.1.2) and the Module to Host (A.2.2.1.3) Are handled by hardware, all other transactions are handled by the uP, using Status and Command registers. In addition, uP can access the Attribute Memory and Configuration Option Register required by PC Card Standard for configuration purposes. This interface works only in 3.3 V mode as defined by [3].

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Register Description

Name	Mode	Offset	Bit	Field Name	Description
Host data	R/W	0	7:0	Data Register	Read and Write port from/to Host
Command	R/W	1	7:0	Command Register	CI Command register
Status	R/W	2	7:0	Status Register	CI Status register
Size Register	R/W	3	15:0	Size Register	CI Size register
HI Status	R	4	7:0		Host Interface Status register (4)
	R		0	--	
	R		1	--	
	R		2	Cmd change	CI Command register changed
	R		3	Host Wr Err	Host Write -> uP Read
	R		4	Host Rd Err	Host Read <- uP Write
	R		5	Host Wr Fifo NE	Fifo data from Host not Empty
	R		6	Host Rd Fifo NE	Fifo data to Host not Empty
	R		7	SRESET	PC Card Soft Reset (1)
HI Interrupt control	W	5	7:0		Host Interface Interrupt control register
	W		0	--	
	W		1	--	
	W		2	Cmd change Inten	CI Command register changed Int Enable
	W		3	Host Rd Err Inten	Host Write Error Int Enable
	W		4	Host Wr Err Inten	Host Read Error Int Enable
	W		5	SRESET Inten	SRESET Int Enable (1)
HI Control	W	6	7:0		Host interface control register
	W		0	CI Interface Clear	Global Host interface clear command
	W		1	FIFO & data Clear	Interface clear command, to be issued by uP when received a RS command (5)
	W		2	READY	READY signal to PC Card Host (2)
Config. Option registers	R	40H	7:0	Config. Option registers	18 bytes of Configuration Option Register. (3)

1. See [3] PC Card Standard 4.13. SRESET is bit 7 of Configuration Option Register 0.
2. See [3] PC Card Standard 4.4.6. Ready pin correspond to the IREQ# pin, deasserted during power up and before PC Card configuration is completed. This signal allows FPGA programming after power up. This functionality is defined only for future use. Alternatively, this FPGA pin can be left unconnected, and the READY can driven by a uP general purpose I/O.
3. Only 4 FCR Configuration Option Registers are implemented (see [3] 4.12.4) :
 Configuration Option Register 0
 I/O Base 0
 I/O Base 1
 I/O Limit
4. The Cmd change flag , register bit 2, is cleared when Cmd change Inten is '0'.
 SRESET follows directly the SRESET bit 7 of Configuration Option Register 0 (see [3] 4.13.1)
 All other bits are errors, cleared only by a reset operation.
5. see [2] 50221.1997 Common interface specification (A.2.2.1.1).

Table 5

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PC Card Attribute memory (CIS)

Name	Mode	Offset	Bit	Field Name	Description
Attribute Memory	RW	0	7:0	Attribute Memory	256 bytes of Attribute Memory (CIS)

- See [3] PC Card Standard. The attribute memory Card Information Structure CIS. At release time will contain a default value, but can be written by uP if needed. During initial debug phase, MUST be written by uP.

Table 6

CIS memory uses 1 FPGA BRam

Bus timing

In order to allow a 5 Volt operation on PC card, all I/O signal between the PC card connector an FPGA MUST be buffered.

For Data bus, a bidirectional buffer with 3-STATE outputs, like 74LCX245 should be used.

In order to minimize external logic, the N_DRV_EN signal is provided this signal can be used to control the direction of data buffer.

The following figure shows the timing of N_DRV_EN signal.

The N_DRV_EN is asserted low when the internal flag READY = '1' and PC Card pin N_CE1 = '0' and PC Card pins N_IORD = '0' or N_OE = '0'.

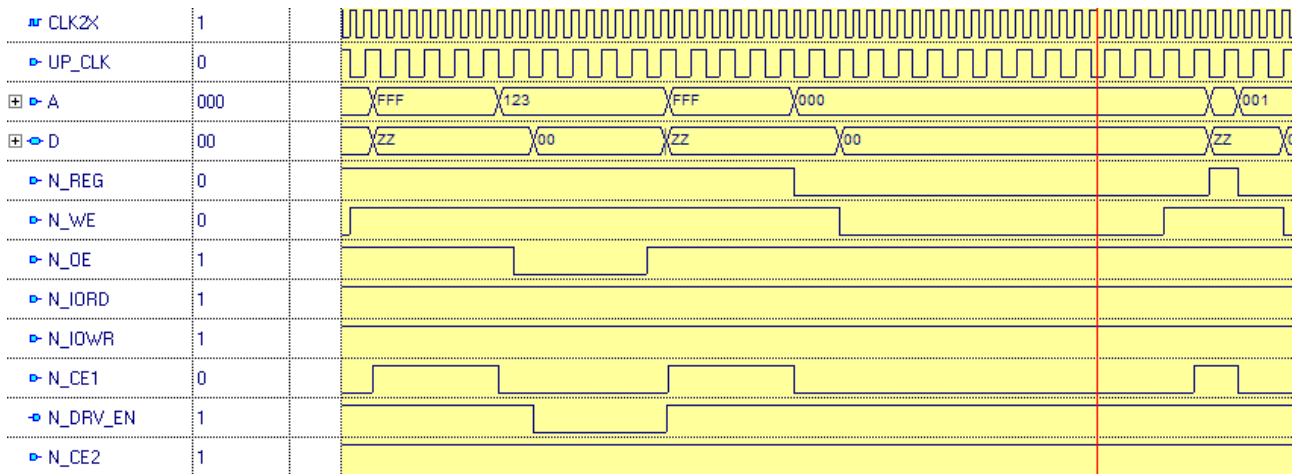


Figure 5

Figure 5 shows the post layout timing for a typical PC Card data cycle.

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MPEG-2 INTERFACE

The MPEG-2 interface includes two different block functions: Filter Block and Descrambler Block.

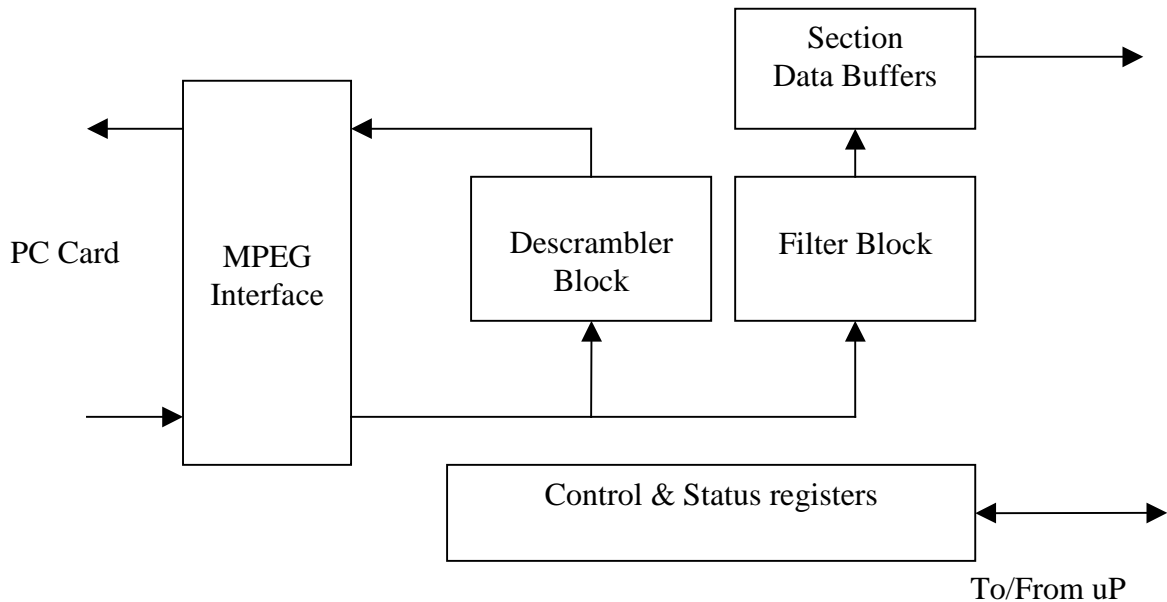


Figure 6

There is one Descrambler Block and one Filter Block composed by 8 filter sections.

The 8 filter sections share a total of 16 elementary filters, which are made by a 64 bit filter pattern register, a 64 bit filter mask register and a control register.

Each filter section has also a 2x512 byte (double) Data Buffer, based on dual port RAM memory, enabling a concurrent read/write operation between filter logic and uP.

FILTER BLOCK

Registers address map

Offset	Mode	Size (bit)	Description
000 to 00F	R/W	32	PID registers 0 to 7 Each register uses 2 memory location
010 to 01F	R/W	32	free
020 to 03F	R/W	16	Filter Control register 0 to 15 Each register uses only the even memory location
040 to 07F	R/W	64	Filter Pattern register 0 to 15 Each register uses 2 memory location
080 to 0BF	R/W	64	Filter Mask register 0 to 15 Each register uses 2 memory location
0F0	R/W	16	Bank and Section Select register
0F1	W	16	Freeze Command byte
0F2	W	16	Read Acknowledge byte
0F4	R/W	16	Interrupt Enable flags

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0F1	R	16	Data Available status flags
0F2	R	16	Data Full status flags
0F3	R	16	Data Overflow flags
0F5	R	16	Data Count for selected Section and Bank
0F6	R	16	End of Transport Packet Data status flags

Table 7

Register Description

Name	Mode	Offset	Bit	Field Name	Description
PID Register 0	R/W	00H	31:0		PID Filter Register #0 (2)
			12:0	PID	PID Value
			18:13	FEF	First Elementary Filter pointer
			19	PIDV	PID Valid (5)
			20	SFEN	Section Filtering Enable
...		PID Filter Register n
PID Register 7	R/W		31:0		PID Filter Register #7
Filter Pattern 0	R/W	40H	63:0		64 bit Filter pattern #0 (3)
...
Filter Pattern 15	R/W	7FH	63:0		64 bit Filter pattern #15 (3)
Filter Mask 0	R/W	80H	63:0		64 bit Filter mask #0
...
Filter Mask 15	R/W	BFH	63:0		64 bit Filter mask #15
Filter Control 0	R/W	20H	15:0		Filter Control Word #0 (3)
			6:0	NEF	Next Elementary Filter pointer
			7	EFEN	Elementary Filter Enable (6)
			8	NC	Next/Current elementary filter (7)
			9	LEF	Last Elementary Filter (9)
...		Filter Control n
Filter Control 15	R/W	3FH	15:0		Filter Control Word #15 (3)
Bank & Section Sel	R/W	F0H	15:0		Select Bank and Section (1)
			2:0	SECTION_SEL	Select the Section to work on
			15:8	BANK_SEL	Select Bank to work on
Freeze Command	W	F1H	7:0	FREEZE_CMD	Freeze Command byte (4)
Read Acknowledge	W	F2H	7:0	ACK_CMD	Read Acknowledge byte (8)
Interrupt Enable	R/W	F4H	15:0		Interrupt Enable Flags
			7:0	INTEN_DF	Data Full Enable, any bank
			15:8	INTEN_DA	Data Available Enable, any bank
Data Available	R	F1H	15:0		Data Available status flags
			7:0	D_AVAIL_0	Data Available flags, Bank 0
			15:8	D_AVAIL_1	Data Available flags, Bank 1
Data Full	R	F2H	15:0		Data Full status flags
			7:0	D_FULL_0	Data Full flags, Bank 0
			15:8	D_FULL_1	Data Full flags, Bank 1
Data Overflow	R	F3H	7:0	D_OVFL	Data Overflow, any bank
Data Count	R	F5H	8:0	DATA_CNT	Data Counter (10)
EOTP	R	F6H	15:0		End of Transport Packet Data status flags
			7:0	EOTP_0	EOTP flags, Bank 0
			15:8	EOTP_1	EOTP flags, Bank 1

1. The Bank & Section Sel register allows to select the Filter Section to work on (from 0 to 7) and the Filter Bank for all sections (there are only two data bank for each section).
2. There are 8 filter sections, which correspond to 8 PID registers and 8 data buffers
3. Each Filter Patter has a correspondent Filter Control register
4. Freeze Command works on all Filter Section at the same time. It force the filter write logic to bank switch.

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5. When '1' the PID compare is forced true:
in this case the PID bits in Control and Mask registers **MUST NOT MASKED OUT**.
6. Controls only filtering, the trigger function is unaffected.
7. When NC is '1' this filter control follow the previous on the same Transport packet
8. Read Acknowledge for Selected Bank, all Sections.
9. This bit should be set if this filter is the last for a given Ts.
10. This register contains the Buffer's data count of the selected Section and Bank.
Each Section buffer is 512 long.

Table 8

Filter Block uses:

512 byte fifo x 2 bank = 1024 byte x 8 Section = 8K byte = 4 BRAM